Electro-mechanical Hybrid PLL

Jakub Gronicz(1) Nikolai Chekurov(2) Lasse Aaltonen(3) Marko Kosunen(1)
Kari Halonen(1)

(1) Aalto University,
School of Electrical Engineering
SMARAD2-Department of Micro and Nanosciences
Espoo, Finland
(2) KTH Royal Institute of Technology
Stockholm, Sweden
(3) Murata Electronics Oy,
Vantaa, Finland

Abstract

This paper describes the design of a double Phase-Locked Loop system that utilizes a MEMS VCO, whose frequency is controlled by means of DC bias. System-level considerations are given for the use of such structure in temperature compensation mechanism for MEMS reference oscillators. A prototype structure (excluding MEMS VCO) has been implemented using a 0.35 μm CMOS process and operates with a nominal supply of 3V.

1 Introduction

Micromechanical resonators offer a viable alternative for replacing quartz in mid to high-grade frequency references e.g. clock sources for signal processing or communication systems [1]. MEMS oscillators provide high quality signal and have been reported to meet GSM phase-noise performance requirements [2]. Along with small form factor and compatibility with CMOS process they are an interesting solution towards a fully integrated frequency reference. Their main flaw however is the strong temperature dependency of the oscillation frequency.

The purpose of this work is to investigate a frequency synthesizer that could address the temperature compensation issues related to both phase noise performance and power consumption in MEMS-based oscillators. The topology investigated in this paper aims to allow for the development of a temperature compensation system that is not tied to any specific MEMS reference resonator structure and does not significantly compromise the output signal quality even for frequencies in the MHz range. While generating frequencies in the GHz range allows for small component sizes, successful implementation of high quality references for frequencies on the order of several or tens of megahertz usually requires the use of either quartz crystals or bulky tank components thus not being feasible for on-chip implementation.

2 System Level Design

The system comprises of two Phase-Locked Loops, as shown in Fig. 1. The double loop approach was motivated by the relatively poor tunability of high-Q MEMS reference resonators which makes direct DC-bias tuning for temperature compensation impractical. Such a solution also requires the reference resonator to have both high Q value and wide tuning range [3]. The double loop approach relaxes the latter requirement allowing high-Q structures to be compensated.

The complete temperature compensation system should comprise of temperature measurement block, a look-up table to store frequency adjustment coefficients, and a PLL responsible for correcting the output frequency according to temperature changes. The output frequency of a PLL $f_{out}$ depends on the divider $N$ and the reference frequency $f_{ref}$ as: $f_{out} = f_{ref} \cdot N$. 

---

XXXIII Finnish URSI Convention on Radio Science and SMARAD Seminar 2013
If the temperature dependency of the reference oscillator is characterized in advance, it can then be used for real-time compensation of the output frequency. The use of a MEMS resonator as a VCO has the potential to improve the noise performance of the entire synthesizer and allow to generate high quality temperature independent signal with low power consumption. As the MEMS VCO operates in closed loop its temperature-related frequency variations will be compensated for by the loop. This also relaxes the requirements on its tuning range which should only be sufficient to cover the process and temperature related frequency shifts of the MEMS VCO.

Temperature compensation of the reference oscillator can then be performed by adjusting the loop division ratio $N$ and if necessary the frequency multiplication factor $M$ of the CMOS PLL.

The MEMS PLL topology is based on a typical charge-pump PLL (Fig. 1) consisting of a digital phase-frequency detector (PFD), charge pump (CP), low-pass loop filter, voltage controlled oscillator (VCO) and an integer frequency divider ($\frac{1}{N}$). The outer loop utilizes a silicon tuning fork-based VCO and has been designed to be very slow thus allowing for more accurate noise filtration. The choice of the low loop bandwidth is supported also by the assumption that the ambient temperature changes smoothly thus fast settling can be sacrificed for the sake of better noise performance that is allowed by the MEMS VCO.

The inner loop acts solely as a frequency multiplier and is implemented as a fast all-electrical CMOS PLL. The bandwidths of inner and outer loop have been chosen to be well over 10 times apart to ensure that their dynamics do not affect each other. The key design parameters of the system are summarized in Table 1a.

### 3 MEMS-based VCO

The VCO is one of the key circuit blocks in the proposed system. It needs to provide high quality output signal and be sufficiently tunable to allow compensating for its own temperature drift and process variations. The use of MEMS-based circuit was enabled mainly by the fact that the technology allows the implementation of high quality, tunable silicon resonators with small size even for MHz frequencies [4].

#### 3.1 Tuning Fork

The resonator structure has been optimized to achieve maximum motional current while maintaining a relatively low tuning voltage. High tunability requirement contributed to the choice of a Clamped-Free (C-F) structure. Assuming the same component size, C-F resonators offer lower mechanical spring constant than e.g. Clamped-Clamped (C-C) or Bulk Acoustic Wave (BAW) [5].
Table 1: System parameter summary.

(a) PLL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output frequency</td>
<td>17.76 MHz</td>
</tr>
<tr>
<td>Tuning range</td>
<td>2364 ppm</td>
</tr>
<tr>
<td>Loop order</td>
<td>2</td>
</tr>
<tr>
<td>Inner Loop BW</td>
<td>30 kHz</td>
</tr>
<tr>
<td>Outer Loop BW</td>
<td>97 Hz</td>
</tr>
<tr>
<td>MEMS VCO gain</td>
<td>9 kHz/V</td>
</tr>
<tr>
<td>Division ratios N,M</td>
<td>12</td>
</tr>
</tbody>
</table>

(b) Tuning fork

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_0$</td>
<td>1.54 MHz</td>
</tr>
<tr>
<td>$\Delta f$</td>
<td>10000 ppm</td>
</tr>
<tr>
<td>$\Delta V_{bias}$</td>
<td>12 V</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>24 V</td>
</tr>
<tr>
<td>beam width $w$</td>
<td>800 nm</td>
</tr>
<tr>
<td>structure thickness $h$</td>
<td>2.5 $\mu$m</td>
</tr>
<tr>
<td>resonator-electrode gap $d$</td>
<td>770 nm</td>
</tr>
</tbody>
</table>

The resonance frequency $f$ can be described as:

$$f = f_0 \left(1 - \sqrt{\frac{k_e}{k_m}}\right),$$

where $f_0$ is the mechanical resonance frequency and $k_m, k_e$ are mechanical and electrical spring constants, respectively. The DC bias tuning is then performed by adjusting $k_e$, which relates to DC voltage $V_{bias}$ as:

$$k_e = \frac{C_0 V_{bias}^2}{d^2},$$

$C_0$ being the electrode capacitance and $d$ – the resonator gap size. Assuming a certain operating frequency, gap size (determined by process limitations) and DC bias voltage, the component size has to be minimized in order to achieve highest motional current.

The tuning fork used in this system has a DC bias lower than 20 V and achieves tunability of more than 10000 ppm over the $V_{bias}$ range of 12 V with respect to the center frequency of 1.54 MHz. The standalone resonator measurements have been performed as it operated in linear region. The structure has been manufactured in a SOI technology using a rapid-prototyping MEMS process. The fabrication allows to obtain functional components within a few hours time. It requires Ga$^{+}$ FIB patterning, cryogenic DRIE, Al evaporation and ALD deposition of thin Al$_2$O$_3$ coating. The SEM image of the resonator is presented in Fig. 2b and its parameters are summarized in Table 1b.

3.2 Oscillator Electronics

The oscillator has been implemented using off the shelf discrete components. The loop amplifier in Fig. 2a provides the necessary gain and phase shift for the oscillations to start.

The first stage of the loop amplifier, $G_1$ is a trans-impedance amplifier, and a biasing circuit for the read-out side of the resonator. Contrary to the drive side, which is biased through a 100 k$\Omega$ resistor, it is more beneficial to bias the read electrode directly using the virtual ground of the amplifier. This minimizes the impact of the parasitic capacitance $C_p$, which would otherwise create a divider with a DC block capacitor and drastically reduce the available signal.

The following four gain stages $G_2, \ldots, G_5$ have two functions. They carry out signal amplification and modify the loop transfer function so that oscillation conditions are fulfilled for the resonant frequency of the MEMS tuning fork.

The current, discrete-component realization of the oscillator makes it less favorable to implement a successful ALC (Automatic Level Control) circuitry, as the driving signal should ideally be limited to 1.5 mVpp. Such block, however is a crucial point of the on-chip implementation of the oscillator which follows in the further development of the presented system.
4 Conclusions

This topology has the potential to be used in a temperature compensation scheme for a MEMS-based frequency reference oscillator. The MEMS VCO being the crucial point from the system performance standpoint, needs to be carefully optimized. Improving the MEMS VCO output signal quality requires designing of an accurate automatic level control circuitry for limiting the oscillator loop gain.

Acknowledgments

The project has been funded by the Academy of Finland (project no. 134506).

References


